REMARKS

Claims 1-74 are now pending in the application. Applicants would like to thank the Examiner for the courtesy extended during the personal interview conducted on February 22, 2006. During the interview, Applicants' representative and the Examiner discussed the Examiner's position regarding the cited art. The Examiner clarified his interpretation of the term "encoded address." The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

Applicant respectfully asserts that the double patenting rejection is premature since neither application has issued.

REJECTION UNDER 35 U.S.C. § 102

Claims 1-5, 8-18, 21-26, and 49-74 are rejected under 35 U.S.C. § 102(b) as being anticipated by Jaggar U.S. Pat. No.5,701,493. This rejection is respectfully traversed.

Jaggar does not show, teach, or suggest a memory unit having a plurality of registers addressable by an encoded address, wherein the encoded address corresponds to a respective one of the plurality of registers and a corresponding processor mode.

For anticipation to be present under 35 U.S.C §102(b), there must be no difference between the claimed invention and the reference disclosure as viewed by one skilled in the field of the invention. *Scripps Clinic & Res. Found. V. Genentech, Inc.*, 18 USPQ.2d 1001 (Fed. Cir. 1991). All of the limitations of the claim must be

inherent or expressly disclosed and must be arranged as in the claim. *Constant v. Advanced Micro-Devices, Inc.*, 7 USPQ.2d 1057 (Fed. Cir. 1988). Here, Jaggar fails to disclose the limitation of a memory unit having a plurality of registers addressable by an encoded address.

FIG. 1 of Jaggar discloses a decoder 17. The decoder 17 receives a composite register address that is a combination of an address from an instruction decoder 14 and a processor mode from a processing status register 18. The decoder 17 compares the composite register address with stored addresses to determine a register address. (Column 2, Lines 24-33). In other words, the decoder 17 first decodes the composite register address and addresses the registers R0, R1, R2,..., R15pc with the decoded address. The registers R0, R1, R2,..., R15pc are addressable by the decoded address, and are not addressable by an encoded address because the decoder 17 must first decode the composite register address. (Column 4, Lines 7-12).

In contrast, Applicants' invention is directed to a registers that are addressable by an encoded address. For example, an exemplary embodiment of the invention as shown in FIG. 6 illustrates a register file memory unit 600. The memory unit 600 includes a plurality of registers. (Paragraph [0047]). Inputs to the memory unit 600 (and therefore the plurality of registers) are encoded addresses, which are outputs of the address encoders 602 and 610. In other words, the plurality of registers comprising the memory unit 600 are addressable by an encoded address. Jaggar fails to show, teach, or suggest this structure. Applicants respectfully submit that claim 1, as well as its dependent claims, should be allowable for at least the above reasons. The remaining claims should be allowable for at least similar reasons.

REJECTION UNDER 35 U.S.C. § 103

Claims 6-7 and 19-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Jaggar in view of Meier et al., U.S. Pat. No. 6,363,471. Claims 27-48 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Jaggar in view of Kerr et al., U.S. Pub. No. 2003/0159021. These rejections are respectfully traversed.

Jaggar, singly or in combination with Meier or Kerr, does not show, teach, or suggest a memory unit having a plurality of registers addressable by an encoded address, wherein the encoded address corresponds to a respective one of the plurality of registers and a corresponding processor mode.

It is a longstanding rule that to establish a prima facie case of obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 180 USPQ 143 (CCPA 1974), see MPEP §2143.03. Furthermore, when evaluating claims for obviousness under 35 U.S.C. §103, all of the limitations must be considered and given weight. *Ex parte Grasselli*, 231 USPQ 393 (Bd. App. 1983), MPEP § 2144.03. Here, it is clear that the Examiner has given little or no consideration of the limitation "a plurality of registers addressable by an encoded address" **and failed to give the limitation any weight.**

FIG. 1 of Jaggar discloses a decoder that compares a composite register address with stored addresses to determine a register address. (Column 2, Lines 24-33). The decoder 17 first decodes the composite register address and addresses the registers R0, R1, R2,..., R15pc with the decoded address. The registers R0, R1, R2,...,

R15pc are addressable by the decoded address, and are not addressable by an encoded address because the decoder 17 must first decode the composite register address. (Column 4, Lines 7-12). Applicants respectfully submit that claims 6-7, 19-20, and 27-48 should be allowable for at least the above reasons.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

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